

ABSTRACT OF THE DISCLOSURE

The present invention relates to a flip-flop circuit employing an MTCMOS technology comprising a master latch unit and a slave latch unit, for latching input data and outputting the data under the control of an internal clock signal, wherein an output of the flip-flop circuit retains a state just before the admission to sleep mode when the state of the system is converted from sleep mode to active by means of making a data state of an input terminal of a master latch circuit into the same state as an inversed data state of an input terminal of a slave latch circuit in sleep mode and storing it.

The flip-flop circuit employing the MTCMOS technology in accordance with the present invention is capable of retaining a state just before the sleep mode when the state of the system is converted from sleep mode to active mode by using the sleep mode control signal by means of adding the feedback circuit to the conventional flip-flop circuit. In addition, while the flip-flop circuit employing the MTCMOS technology in accordance with the present invention has an operation speed slightly slower than that of the prior art flip-flop circuit employing the low-V_{th} transistor or the high-V_{th} transistor, a leakage current of the present invention is significantly smaller than that of the conventional art.